[METHOD, SYSTEM AND APPARATUS FOR AGGREGATING FAILURES ACROSS MULTIPLE MEMORIES AND APPLYING A COMMON DEFECT REPAIR SOLUTION TO ALL OF THE MULTIPLE MEMORIES]

Abstract

An integrated circuit includes a plurality of separate memory arrays each having a respective one of a plurality of inputs and a respective one of a plurality of outputs. Each output provides an output value indicative of whether a storage location associated with an applied address is passing or failing. The integrated circuit further includes a shared built-in self-test (BIST) and repair system coupled to all of the plurality of inputs and all of the plurality of outputs. The shared BIST and repair system applies addresses and data to the plurality of inputs to test the plurality of memory arrays for failing storage locations. In response to detection of a failing storage location in any of the plurality of memory arrays, the shared BIST and repair system applies a common address remapping to all of the plurality of memory arrays to remap, in each memory array, the address associated with the failing storage location to a different storage location